

Physical Model for GaN HEMT Design Optimization in High Frequency Switching Applications

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Abstract—In this paper, physical modeling of a GaN HEMT is proposed, with the objective of device design optimization for application in a high frequency DC/DC converter. From the point of view of a switching application, physical model for input, output and reverse capacitance as well as for channel resistance is very important, since the aforementioned parameters determine power losses in the circuit. The obtained physical model of the switching device can be used for simulation models such as PSpice or hybrid behavioral power loss models for high frequency DC/DC converters. In this work, extrinsic model for I_d (V_{ds} , V_{gs}) output characteristics of a depletion mode GaN HEMT with a field plate structure was obtained, as well as physical model for input, output and reverse capacitance in the subthreshold regime. The model was implemented in Simplorer simulation model and verified by the measured efficiency curves of the buck converter prototype, using the GaN HEMT that was analyzed. With the increase of the switching frequency, precision of the model increases, especially in the low power area, which is the area of interest in our application.

Keywords—GaN HEMTs; physical modeling; output characteristics, parasitic capacitances

I. INTRODUCTION

GaN based High Electron Mobility Transistors (HEMTs) are the most promising switching devices for high frequency applications [1]. Comparing to corresponding Si devices, their superior conductivity and switching characteristics give several times better Figure Of Merit [2], [3]. A significant progress in GaN HEMT design has been made, providing higher breakdown voltages and lower gate leakage currents by application of the field plate structure [4]. Also, big effort was made in the analysis of dynamic on-resistance and corresponding trapping effects [5].

High frequency DC/DC converter can be applied as a dynamic power supply for Radio Frequency Power Amplifier in Envelope Tracking and Envelope Elimination and Restoration Techniques. The topology that was considered in our work is a synchronous buck converter (Fig. 1) with GaN HEMTs employed as switching devices. Since wide bandwidth is a crucial feature of the converter, high switching frequency is needed. This implies importance of the physical model for input, output and reverse capacitance of the device,

since they determine switching power losses and limit the switching speed. On the other hand, since the switching device operates in a linear part of the output characteristics, a model for on-resistance is necessary since this parameter determines conduction losses in the circuit. In order to obtain the relation between the power losses and switching device design, physical model is necessary. This was the main motivation in our work.

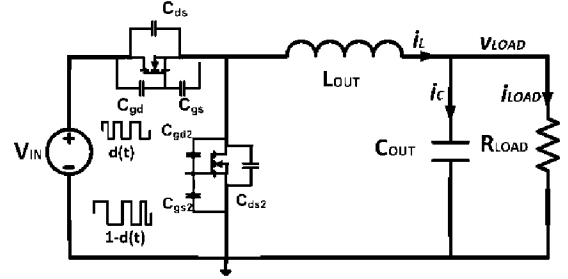


Fig. 1. Synchronous buck converter with applied switching devices

II. 2 DEG SHEET DENSITY DEPENDENCE ON THE APPLIED GATE VOLTAGE

The starting point for the physical model of a GaN HEMT is the charge control by the Schottky gate. Assuming that the 2DEG is being formed in a triangular quantum well, with only the first two subbands E_0 and E_1 possibly occupied, the 2DEG can be presented using Fermi-Dirac statistics as [6]

$$n_{2DEG} = D k_B T \left[\ln \left(1 + e^{\frac{(E_F - E_0)}{k_B T}} \right) + \ln \left(1 + e^{\frac{(E_F - E_1)}{k_B T}} \right) \right] \quad (1)$$

where n_{2DEG} is the 2DEG sheet density, $D = 4\pi m_{le}^* / h^2$ is the density of states for each subband, k_B is the Boltzmann's constant, m_{le}^* is the longitudinal effective mass of electron ($= 0.22m_e$ with m_e as the electron mass), h is the Planck's constant, T is the temperature and E_F is the Fermi energy. The aforementioned subbands E_0 and E_1 are related to the 2DEG density as: $E_0 = \lambda_0 n_{2DEG}^{2/3}$, $E_1 = \lambda_1 n_{2DEG}^{2/3}$ in (eV), with $\lambda_0 = 2.123 \cdot 10^{-12}$ and $\lambda_1 = 3.734 \cdot 10^{-12}$ [6].

If we assume that gate and heterojunction depletion areas are overlapped resulting in total depletion of AlGaIn layer, we can apply Poissons equation to AlGaIn and GaN layer, together with Gauss's law for charge conservation at the AlGaIn/GaN

heterojunction (Fig. 2). This results in the following equation for 2DEG sheet density, n_{2DEG} :

$$n_{2DEG} = \frac{\varepsilon_a(m)}{q(d_d + d_{sp})} \left(V_g - V_{th}(m) - \frac{E_F}{q} \right) \quad (2)$$

where m is the Al mole fraction in $Al_mGa_{(1-m)}N$, $\varepsilon_a(m)$ is the permittivity of $Al_mGa_{(1-m)}N$, d_d and d_{sp} are the thickness of doped and spacer layer in AlGaN, respectively, V_g is the applied gate voltage and V_{th} is the threshold voltage given by the following equation

$$V_{th}(m) = \phi_s(m) - \Delta E_C(m) - \frac{qN_D d_d^2}{2\varepsilon_a(m)} - \frac{\sigma_{PZ}(m)}{\varepsilon_a(m)}(d_d + d_{sp}) \quad (3)$$

In the previous equation, $\phi_s(m)$ is the height of the Schottky barrier at gate-AlGaN heterojunction (1.165V), $\Delta E_C(m)$ is the conduction band discontinuity at the AlGaN/GaN interface (the height of the quantum well) equal to 0.343V while $\sigma_{PZ}(m)$ is the polarization-induced charge density of $0.0105C/m^2$ and is calculated using [6]. For the analyzed GaN HEMT, Eq. (3) gives a threshold of -2.0899V which is in good agreement with the measured value of -2V. In order to obtain the Fermi level dependence on the applied gate voltage, model from [7] was used to approximate (1) for different relative positions of E_F , E_0 and E_1 . In that way, the 2DEG dependence on the gate voltage is obtained and presented in Fig 3.

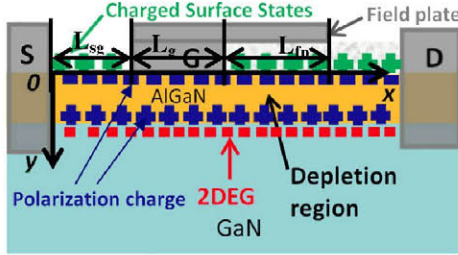


Fig.2. Cross section of a GaN HEMT with a field plate

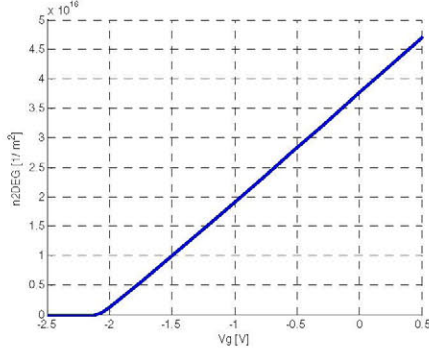


Fig. 3 2DEG sheet density control by the gate voltage, for $V_{ds}=0$

W_g [mm]	L_g [um]	L_{sg} [um]	L_{fp} [um]	t_{ox} [nm]	d_d [nm]	d_{sp} [nm]	m [%]	N_d [1/m ³]
120	2	2	1.5	80	20	3	25	10^{22}

Table 1. Parameters of the analyzed GaN HEMT with SiN field plate structure

III. MODELING OF EXTRINSIC OUTPUT CHARACTERISTICS

With 2DEG sheet density dependence on the gate voltage completed, it is possible to obtain the extrinsic $I_d(V_{ds}, V_{gs})$ output characteristics of the HEMT. The drain current is modeled as [6]

$$I_d = q W_g v_{DRIFT}(x) n_{2DEG}(x) \quad (4)$$

where q is electron charge, W_g is the gate width and $v_{DRIFT}(x)$ is the electron velocity given by

$$v_{DRIFT}(x) = \frac{\mu_0}{1 + \frac{E(x)}{E_C}} E(x) \quad \text{for } E(x) < E_C \quad (5a)$$

$$v_{DRIFT} = v_{SAT} \quad \text{for } E(x) > E_C \quad (5b)$$

In (5a), $E(x) = -dV_c(x)/dx$ is the lateral electric field at any point x in the channel, $V_c(x)$ is the channel potential, μ_0 is the low field mobility of 2DEG and is approximately equal to 1000 cm²/Vs, E_C is the critical electric field and v_{SAT} is the saturation velocity of 3.775×10^5 m/s. For linear region of operation we derive the expression for the drain current by solving (4) under the boundary conditions: $V_c(x=L_{sg})=I_d(R_{s,cm}+R_{s,drift})$ and $V_c(x=L_{sg}+L_g)=V_{ds}-I_d(R_{d,cm}+R_{d,drift})$. In the previous calculation, $R_{s,cm}$ and $R_{d,cm}$ are contact and metallization resistances of source and drain (approximately 25mΩ each), while $R_{d,drift}$ and $R_{s,drift}$ are drain and source drift resistances and they are modeled as

$$R_{D,DRIFT} = \frac{L_{gd}}{q\mu_0 W_g n_{s0}}; \quad R_{S,DRIFT} = \frac{L_{gs}}{q\mu_0 W_g n_{s0}} \quad (6a, b)$$

In (6a, b) n_{s0} is equal to the value of the 2DEG in the drift regions between source and the channel, and drain and the channel. This value corresponds to the value of 2DEG sheet density for gate voltage of zero volts. For the given geometry, we obtain $R_{d,drift}=54.8m\Omega$ and $R_{s,drift}=27.4m\Omega$.

The onset of saturation is defined when the electric field at the drain end of the channel (at $x_1=L_{sg}+L_g$) reaches the critical value E_C while the electron velocity reaches v_{SAT} . For drain voltages that are exceeding V_{dsat} , the point of saturation will move from the drain end (the point x_1) towards source contact and the saturation current was modeled taking into account this channel length modulation [8]. The obtained extrinsic output characteristics are shown in Fig. 4. Observing the comparison with the experimental characterization of the device, it can be seen that the highest error of approximately 32% was found deeply in the saturation area, most likely due to additional effect of the field plate structure on the channel length modulation, which was not taken into account in the model. In the linear region, which is the area of interest for a switching application, a good agreement between the model and the measurements is observed.

IV. MODELING OF INPUT, OUTPUT AND REVERSE CAPACITANCE

As it was already mentioned, dependences of input, output and reverse capacitance on drain-to-source voltage when the transistor is in the off-state (V_{gs} below the threshold value), are very important for the design of switching devices in high frequency applications.

In order to find the origin of Millers capacitance (C_{gd}), we will observe the simulation of the 2DEG distribution in the channel, for $V_{gs}=-3V$ and V_{ds} being changed from 10 to 60V (Fig. 5). It can be seen, that the main part of 2DEG leftover under the field plate is being depleted for V_{ds} lower than 20V, caused by the electric field component perpendicular to the channel, E_y . On the other hand, lateral component of the electric field will provide additional extension of this depletion area in the whole range of V_{ds} . The simulation of the

lateral component of the electric field, E_x , is presented in Fig. 6. In order to physically model 2DEG depletion process under E_y component, the following methodology was proposed. Since V_{gs} is constant and V_{ds} is being changed, the metal-insulator-semiconductor structure has been analyzed and its 2DEG sheet density dependence on the V_{gd} was obtained. The closed form solution for this dependence is:

$$n_{2DEG_{FP}}(V_{gd}) = \frac{\sigma_{PZ}}{q} \frac{\epsilon_a - V_{gd} + \phi_b - \Delta E_C + \frac{qN_d((t_{ox} - d_d)^2 - d_{sp}^2)}{2\epsilon_a} + q t_{ox} N_d \frac{(t_{ox} - d_d)}{\epsilon_{ox}}}{t_{ox} \left(1 + \frac{\epsilon_a}{\epsilon_{ox}}\right) - (d_d + d_{sp})} \quad (7)$$

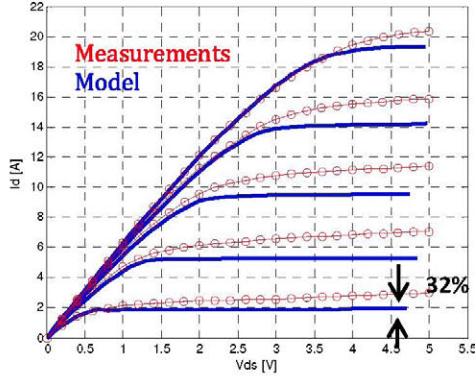


Fig.4. Extrinsic output characteristics of the HEMT: measured -red and modeled -blue

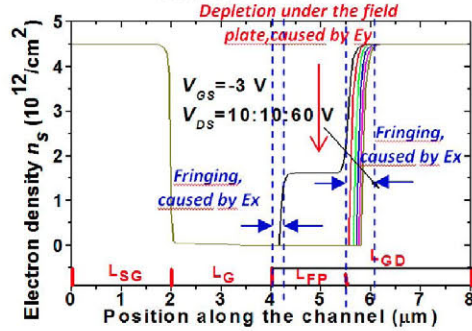


Fig.5. Simulation of 2DEG depletion in the channel, with increase in V_{ds} from 10V (black) up to 60V (green), with a 10V step

In (7), ϕ_b is the metal-insulator barrier height (equal to 2.2V), t_{ox} and ϵ_{ox} are the thickness and permittivity of the field plate. From (7), using $V_{gd} = V_{gs} - V_{ds}$ and $C_{gd}(V_{ds}) = q L_{FP} W_g \frac{dn_{2DEG_{FP}}}{dV_{ds}}$, we obtain the expression for the part of C_{gd} caused by the E_y , C_{gdy} :

$$C_{gdy}(V_{ds}) = L_{FP} W_g \frac{\epsilon_a}{(t_{ox}(1 + \frac{\epsilon_a}{\epsilon_{ox}}) - (d_d + d_{sp}))} \quad (8)$$

For $V_{ds} > 16.5V$, $C_{gdy}(V_{ds}) = 0$. In the case of analyzed HEMT, this value is equal to 96.3pF.

In order to model fringing of the depletion area in x-direction, conformal mapping technique has been used. In that way, depletion area extension dependence on the applied V_{ds} has been obtained. In the range of drain voltages lower than 16.5V, this capacitance is added to the C_{gdy} to obtain total Miller's capacitance, while for higher V_{ds} , this fringing part represents the total C_{gd} . The comparison between the obtained

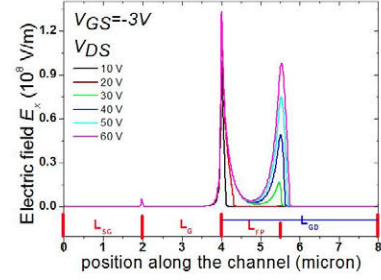


Fig.6. Simulation of lateral electric field in the channel

model and the measurements is presented in Fig.7. It can be seen that the knee voltage has been modeled precisely and that the highest error of 22% is obtained in the fringing area, where the capacitance values have the order of pF.

Speaking of output capacitance, $C_{oss} = C_{gd} + C_{ds}$, it was necessary to determine the capacitance between drain and source terminal of the device. This capacitance mainly depends on the geometry of the device and how the metal layers are placed. In the case of the analyzed transistor, the main part of this capacitance is caused by the fringing between drain and source electrodes through GaN layer and for the given geometry is equal to 40pF.

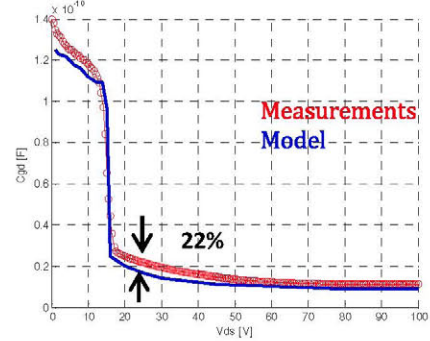


Fig.7. Modeled C_{gd} (blue) versus measurements (red)

Gate to source capacitance also has the origin in the fringing between the electrodes through AlGaIn layer (Fig. 8). The second important source of this capacitance is in the fringing between the metal pads that connect all gate and source fingers through AlGaIn and GaN as well (Fig 9). The aforementioned capacitances have the values of 246 and 97pF, respectively. As it can be seen from Fig. 10, the highest error of 40% in the capacitance model is found in the fringing area of C_{oss} . Nevertheless, in absolute units this error is very small from the point of view of modeled application (HF DC DC converter), as it can be seen later. The modeled nonlinear capacitances are very important because they limit the "turn on/off" speed of the transistor that is used as a switch in this application. The slower the device the higher are the switching losses. Once the transistor is fully turned on, the losses are due to the current conduction and resistance of the metallization, contacts and the channel. The importance of obtained physical model of the device is that, through electrical model, it can be connected to a particular application (in our case HF buck converter) and subsequently, from the minimization of the power losses in the

circuit, the optimization of the device design can be done. In [9], a hybrid behavioral-analytical power loss model for HF buck converter is presented and can be used as the aforementioned connection between the device physics and our application.

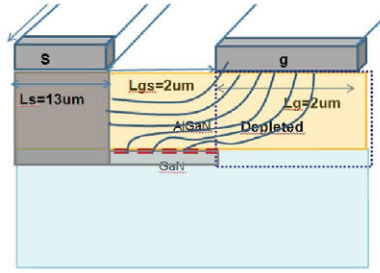


Fig. 8 Fringing between gate and source electrodes

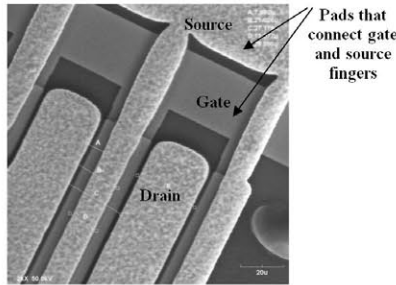


Fig. 9 Fringing between gate and source finger-connecting pads

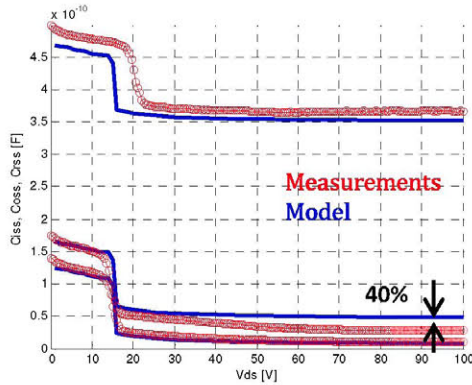


Fig. 10 Complete model versus measurements for C_{iss} , C_{oss} and C_{rss}

In order to verify the proposed physical model, a high frequency buck converter with analyzed GaN HEMT has been built and tested at three different switching frequencies (7, 15 and 20MHz), changing the duty cycle in order to provide different output power levels. Measured efficiency curves are presented in Fig. 11, together with the simulated ones. Simulation was done in Simplorer, using the curves from previously presented physical model. It can be seen that good agreement between the simulation and the measurements has been obtained at each switching frequency.

V. CONCLUSIONS

Physical modeling of a GaN HEMT with field plate structure has been proposed in this paper. Obtained analytical model for

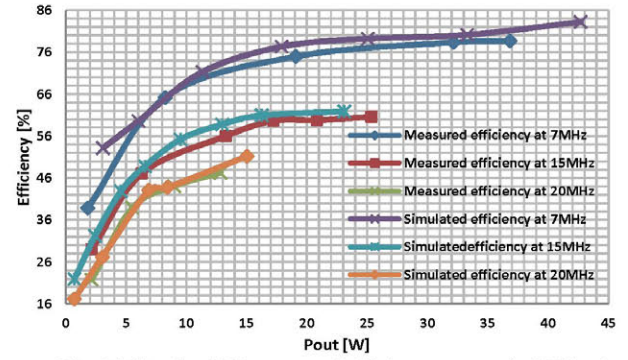


Fig. 11 Simulated Vs measured efficiency curves for HF buck

extrinsic output characteristics showed good agreement with the measurements in a linear part which is the area of interest in a switching application. On the other hand, input, output and reverse capacitance dependence on V_{ds} in subthreshold regime has been obtained. Complete 2DEG depletion process was addressed and modeled. Different parts of the capacitances, caused by fringing between the electrodes and multifinger configuration of the device were established. Using the presented dependencies between the device capacitances and its geometry it is possible to optimize the width and length of the transistor gate, drain and source, and the number of paralleled fingers as well [10]. The obtained physical curves can be related to HF buck converter using hybrid PSpice model from [9]. Measured efficiency curves of a HF buck converter showed good agreement with simulated values at three different switching frequencies and verified the proposed model.

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